CLAIM AMENDMENTS:

Please cancel claim 23, amend claim 28, and add new claims 32-36. A full listing of the claims follows.

23. (Canceled)

24. (Previously presented) A non-volatile memory, comprising:

an array of charge storage elements formed on a semiconductor substrate,

field dielectric material positioned between the charge storage elements in at least one direction across the array, and

electrically conductive control gates extending across tops of the array of charge storage elements in said at least one direction with a layer of dielectric positioned therebetween and protruding downward into slots formed in the field dielectric between adjacent ones of the charge storage elements, the downward portions of the control gates providing electrical shielding between adjacent charge storage elements in said one direction.

25. (Previously presented) The memory of claim 24, wherein the individual charge storage elements have different widths across top and bottom portions thereof in said at least one direction, the top portions being wider than the bottom portions, and the control gates protruding downward therebetween a distance at least as great as a thickness of the top portions.

26. (Previously presented) The memory of claim 24, wherein the field dielectric is formed over a surface of the semiconductor substrate.

27. (Previously presented) The memory of claim 24, wherein the array includes the storage elements arranged in a regular pattern of rows and columns, said at least one direction extending along the columns, and wherein the rows include select

gates and source/drain regions in the substrate alternately positioned between adjacent storage elements along the rows.

28. (Currently amended) A non-volatile memory, comprising:

a rectangular array of charge storage elements formed on a substrate surface with a first layer of dielectric therebetween, the individual charge storage elements including a first portion positioned against the first dielectric layer with a first width in one direction across the array and a second portion integrally formed with the first portion a distance removed from the first dielectric layer and with a second width in said one direction, said second width being greater than said first width, and

elongated electrically conductive control gates extending in said one direction across surfaces of a plurality of charge storage elements furthest removed from the substrate and with a second layer of dielectric therebetween, the control gates additionally extending between adjacent charge storage elements for a distance ~~at least equal to~~ greater than a thickness of the second portion of the charge storage elements, the extensions of the control gates between adjacent charge storage elements providing electrical shielding in said one direction between at least the second portions thereof.

29. (Previously presented) The non-volatile memory of claim 28, wherein dielectric material fills spaces between the first portions of adjacent ones of the charge storage elements and includes a slot therein into which the control gates extend a distance between the first portions of adjacent charge storage elements.

30. (Previously presented) The non-volatile memory of claim 29, wherein the dielectric material between the first portions of adjacent ones of the charge storage elements is formed over the substrate surface.

31. (Previously presented) The non-volatile memory of claim 28, wherein the array includes memory cells that individually include, in a second direction across the array, two charge storage elements between adjacent substrate source and drain regions

and a select transistor between the two charge storage elements, said second direction being perpendicular to said one direction.

32. (New) A non-volatile memory, comprising:

an array of charge storage elements across a substrate surface, individual charge storage elements including a first portion having a first dimension in a first direction and a second portion having a second dimension in the first direction that is greater than the first dimension, the first portion located between the second portion and the substrate surface, the first portion and second portion contacting along a plane; and

a plurality of elongated conductive elements extending in the first direction, an elongated conductive element extending across a plurality of charge storage elements, protrusions of the elongated conductive element extending between adjacent charge storage elements to a level that is closer to the substrate surface than the plane is to the substrate surface.

33. (New) The non-volatile memory of claim 32 wherein the second portion of an individual charge storage unit has an upper surface that extends along the first direction and two side surfaces that are on opposing ends of the second portion in the first direction, the elongated conductive element extending across the upper surface of the charge storage unit and the protrusions of the elongated conductive element extending along the side surfaces.

34. (New) The non-volatile memory of claim 33 wherein the second portion is separated from the elongated conductive element by a dielectric layer.

35. (New) The non-volatile memory of claim 32 wherein the first and second portions are separately formed.

36. (New) The non-volatile memory of claim 32 wherein the first and second portions are formed together by a single process.